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Attorney Docket No. c-6-us c-6-us.tri

These documents are being hand-delivered on or about 5/8/97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventor(s): Eldridge, et al.

Serial No.: 08/554,902 **Examiner: Goins, C.**

Filing Date: 11/09/95 **Art Unit: 3206**

To: Commissioner of Patents and Trademarks
Washington, DC 20231

TRANSMITTAL

Enclosed herewith is:

- SUPPLEMENTAL INFORMATION DISCLOSURE (6)
- SUPPLEMENTAL INFORMATION DISCLOSURE (7)
- SUPPLEMENTAL INFORMATION DISCLOSURE (8)
- copies of references

- SUPPLEMENTAL DECLARATION

The most recent action in this case was an Office action requiring restriction or election, to which a response was filed on **4/4/97**.

These Supplemental Information Disclosure Citations are being hand-delivered, prior to an action on the merits. **NO FEE IS REQUIRED**

If it is determined that a fee is required, the three Supplemental Information Disclosure Citations enclosed herewith should be treated as ONE Information Disclosure Citation.

Charge any shortfall to Dep. Acct. 12-1445

For the Applicant,

Gerald E. Linden 30,282 5/7/97
(407) 382-7966 date

#8
5/9/97 JH

Attorney Docket No. c-6-us c-6-us.id6

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventor(s): Eldridge, et al.

Serial No.: 08/554,902

Filing Date: 11/09/95

SUPPLEMENTAL INFORMATION DISCLOSURE CITATION
(Substitute PTO-1449)

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION (6) is being provided in addition to:

(1) INFORMATION DISCLOSURE CITATION, filed 4/4/96
(2) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(3) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(4) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(5) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 7/17/96

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

Attention is directed to the following commonly-owned patents, **copies of which are enclosed herewith:**

5,476,211 Khandros; 12/95 228/180.5
METHOD OF MANUFACTURING ELECTRICAL CONTACTS, USING A SACRIFICIAL MEMBER

5,601,740 Eldridge, et al.; 2/97 219/130.4
METHOD AND APPARATUS FOR WIREBONDING, FOR SEVERING BOND WIRES, AND FOR FORMING BALLS ON THE ENDS OF BOND WIRES

SOURCES OF THE REFERENCES

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION lists references cited in the International Search Reports pertaining to various commonly-owned, copending PCT applications. All the references listed in the Search Reports are listed herein. However, if the references have previously been disclosed, only the patent number is listed.

The references presented herein are arranged in "groups", as follows:

GROUP 1. These references were cited in:
_x_ the International Search Report
___ the Written Opinion
pertaining to commonly-owned, copending **PCT/US96/08328 filed 28 May 96. [C-8-PCT]**

___ copies of these references are enclosed herewith, except for copies of references previously submitted to the Patent Office;

_x_ copies of these references are NOT enclosed herewith, but have (i) previously been disclosed or (ii) will be supplied to the file of commonly-owned, copending U.S. Patent Application No. **08/602,179 filed 15 Feb 96. [C-8-US]**

GROUP 1A. These references were cited in an Office action pertaining to commonly-owned, copending **08/602,179 filed 15 Feb 96 [C-8-US]**

GROUP 2. These references were cited in:
_x_ the International Search Report
___ the Written Opinion
pertaining to commonly-owned, copending **PCT/US96/07924 filed 24 May 96. [C-9-PCT]**

___ copies of these references are enclosed herewith, except for copies of references previously submitted to the Patent Office;

_x_ copies of these references are NOT enclosed herewith, but have (i) previously been disclosed or (ii) will be supplied to the file of commonly-owned, copending U.S. Patent Application No. **08/340,144 filed 15 Nov 94 [C-2-US]**

GROUP 3. These references were cited in:
_x_ the International Search Report
_x_ the Written Opinion
pertaining to commonly-owned, copending **PCT/US96/08275 filed 28 May**

96. [C-11-PCT]

___ copies of these references are enclosed herewith, except for copies of references previously submitted to the Patent Office;

_x_ copies of these references are NOT enclosed herewith, but have (i) previously been disclosed or (ii) will be supplied to the file of commonly-owned, copending U.S. Patent Application No. **08/749,111 filed 14 Nov 96. [C-11-US]**

GROUP 4. These references were cited in:
_x_ the International Search Report
___ the Written Opinion
pertaining to commonly-owned, copending **PCT/US96/08117 filed 24 May 96. [C-12-PCT]**

___ copies of these references are enclosed herewith, except for copies of references previously submitted to the Patent Office;

_x_ copies of these references are NOT enclosed herewith, but have (i) previously been disclosed or (ii) will be supplied to the file of commonly-owned, copending U.S. Patent Application No. **08/789,147 filed 24 Jan 97. [C-12-US]**

GROUP 4A. References located in a recent search pertaining to comonly-owned, copending U.S. Patent Application No. **08/789,147 filed 24 Jan 97. [C-12-US]**
NOTE: THESE REFERENCES ARE THE SAME AS IN GROUP 5A

GROUP 5. These references were cited in:
_x_ the International Search Report
___ the Written Opinion
pertaining to commonly-owned, copending **PCT/US96/08107, filed 24 May 96. [C-14-PCT]**

___ copies of these references are enclosed herewith, except for copies of references previously submitted to the Patent Office;

_x_ copies of these references are NOT enclosed herewith, but have (i) previously been disclosed or (ii) will be supplied to the file of commonly-owned, copending U.S. Patent Application No. **08/788,740 filed 24 Jan 97. [C-14-US]**

GROUP 5A. References located in a recent search

pertaining to comonly-owned, copending U.S. Patent Application No. **08/788,740 filed 24 Jan 97 [C-14-US]**

GROUP 6. These references were cited in:
_x_ the International Search Report
___ the Written Opinion
pertaining to commonly-owned, copending **PCT/US96/08274, filed 28 May 96. [C-15-PCT]**

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_x_ copies of these references are NOT enclosed herewith, but have (i) previously been disclosed or (ii) will be supplied to the file of commonly-owned, copending U.S. Patent Application No. **08/779,020 filed 10 Feb 97. [C-15-US]**

GROUP 7. These references were cited in:
_x_ the International Search Report
___ the Written Opinion
pertaining to commonly-owned, copending **PCT/US96/08276, filed 28 May 96. [C-16-PCT]**

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_x_ copies of these references are NOT enclosed herewith, but have (i) previously been disclosed or (ii) will be supplied to the file of commonly-owned, copending U.S. Patent Application No. **08/794,202 filed 24 Jan 97. [C-16-US]**

GROUP 8A. These references were found in a database search.

___ copies of these references are enclosed herewith, except for copies of references previously submitted to the Patent Office;

_x_ copies of these references are NOT enclosed herewith, but will be supplied to the file of commonly-owned, copending U.S. Patent Application No. **08/340,144 filed 15 Nov 94 [C-2-US]**

SHOULD THE EXAMINER DESIRE COPIES OF ANY REFERENCES CITED HEREIN, OR IN PREVIOUS INFORMATION DISCLOSURE CITATIONS, APPLICANT WILL PROVIDE SAME UPON REQUEST.

GROUP 1: PCT/US96/08328, filed 28 May 96 **[C-8-PCT]**

5,414,298 Grube, et al.; 5/95 257/690
SEMICONDUCTOR CHIP ASSEMBLIES AND COMPONENTS WITH PRESSURE CONTACT
PREVIOUSLY DISCLOSED

3,842,189 Southgate; 10/74 174/52 S
CONTACT ARRAY AND METHOD OF MAKING THE SAME
PREVIOUSLY DISCLOSED

5,346,861 Khandros, et al.; 9/94 437/209
SEMICONDUCTOR CHIP ASSEMBLIES AND METHODS OF MAKING SAME
PREVIOUSLY DISCLOSED

5,230,632 Baumberger, et al.; 7/93 439/66
DUAL ELEMENT ELECTRICAL CONTACT AND CONNECTOR ASSEMBLY UTILIZING SAME

GROUP 1A: 08/602,179 filed 15 Feb 96 **[C-8-US]**

5,239,447 Cotues, et al.; 8/93 361/744
STEPPED ELECTRONIC DEVICE PACKAGE
PREVIOUSLY DISCLOSED

5,310,702 Yoshida, et al.; 5/94 437/211
METHOD OF PREVENTING SHORT-CIRCUITING OF BOND WIRES

5,481,241 Caddock, Jr.; 1/96 338/51
FILM-TYPE HEAT SINK-MOUNTED POWER RESISTOR COMBINATION HAVING ONLY A THIN ENCAPSULANT, AND HAVING AN ENLARGED INTERNAL HEAT SINK

4,132,341 Bratschun; 1/79 228/122
HYBRID CIRCUIT CONNECTOR ASSEMBLY

5,294,039 Pai, et al.; 3/94 228/180.22
PLATED COMPLIANT LEAD
PREVIOUSLY DISCLOSED

5,346,861 Khandros, et al.; 437/209
SEMICONDUCTOR CHIP ASSEMBLIES AND METHODS OF MAKING SAME
PREVIOUSLY DISCLOSED

Jap. 57-152137 9/82 Saeki (56-35430) 437/209
SEMICONDUCTOR PACKAGE AND MANUFACTURE THEREOF

Jap. 56-26446 3/81 Nakatani (54-101710) 437/209
SEMICONDUCTOR DEVICE

GROUP 2: PCT/US96/07924, filed 24 May 96 **[C-9-PCT]**

3,214,563 Ford; 10/65 219/69
ELECTRICAL DRILLING

4,829,153 Correy; 5/89 219/130.4
WELDING ARC INITIATOR

5,006,688 Cross; 4/91 219/130.4
LASER-ARC APPARATUS AND METHOD FOR CONTROLLING PLASMA CLOUD

5,095,187 previously disclosed to PTO

GROUP 3: PCT/US96/08275, filed 28 May 96 **[C-11-PCT]**

3,636,242 Hansson; 1/72 174/128
AN ELECTRIC CONDUCTOR WIRE

4,537,808 Yamamoto, et al.; 8/85 428/36
ELECTRICALLY CONDUCTIVE COMPOSITE MATERIAL

5,045,410 Hiesbock, et al.; 9/91 428/644
LOW PHOSPHOROUS CONTAINING BAND-SHAPED AND/OR FILAMENTARY MATERIAL

4,354,310 Hatton; 10/82 29/605
METHOD OF MAKING INDUCTANCE

4,025,143 Rozmus; 5/77 339/278C
ELECTRICAL CONTACTS

5,059,143 Grabbe; 10/91 439/886
CONNECTOR CONTACT

5,129,143 Wei, et al.; 7/92 29/885
DURABLE PLATING FOR ELECTRICAL CONTACT TERMINALS

5,163,835 Morlion, et al.; 11/92 439/67
CONTACT ASSEMBLY WITH GROUNDING CONTACT SUPPORT

5,090,119 Tsuda, et al.,; 2/92 29/843
METHOD OF FORMING AN ELECTRICAL CONTACT BUMP

5,172,851 Matsushita, et al.,; 12/92 228/179
METHOD OF FORMING A BUMP ELECTRODE AND MANUFACTURING A RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

GROUP 4: PCT/US96/08117, filed 24 May 96 **[C-12-PCT]**

see PCT search report

IBM Technical Disclosure Bulletin, Vol. 21, No. 8, January
TEXT PROBE CONTACT GRID TRANSLATOR BOARD

IBM Technical Disclosure Bulletin, Vol. 21, No, 4, Sept. 1978
AUTOMATIC TEST EQUIPMENT TRANSLATOR BOARD

IBM Technical Disclosure Bulletin, Vol. 17, No. 2, July 1974
MULTIPOINT TEST PROBE FOR PRINTED CARDS

JP A 54-146581
ELECTRIC CHARACTERISTIC MEASURING DEVICE FOR SEMICONDUCTOR CHIP

4,998,885 Beaman; 3/91 439/66
ELASTOMERIC AREA ARRAY INTERPOSER

4,899,106 Ogura; 2/90 324/158 F
PERSONALITY BOARD

4,724,383 Hart; 2/88 324/158 F
PC BOARD TEST FIXTURE

4,528,500 Lightbody, et al.; 7/85 324/73 PC
APPARATUS AND METHOD FOR TESTING CIRCUIT BOARDS

4,508,405 Damon, et al.; 4/85 339/75 MP
ELECTRONIC SOCKET HAVING SPRING PROBE CONTACTS

4,357,062 Everett; 11/82 339/18 R
UNIVERSAL CIRCUIT BOARD TEST FIXTURE

GROUP 4A: **See GROUP 5A hereinbelow**

GROUP 5: PCT/US96/08107, filed 24 May 96 **[C-14-PCT]**

5,476,211 (See above. commonly-owned patent)

Jap. 3-279370; Otsuka; 9/92 (4-355940)
JOINING METHOD FOR TAB INNER LEAD AND BONDING TOOL FOR JUNCTION

Jap. 63-221924; Hokari; 8/90 (2-69940)
SEMICONDUCTOR INTEGRATED CIRCUIT BONDING PAD CONFIGURATION

GROUP 5A: USSN 08/788,740, filed 24 Jan 97

5,569,272 Reed, et al.; 10/96 606/151
TISSUE-CONNECTIVE DEVICES WITH MICROMECHANICAL BARBS

5,393,375 MacDonald, et al.; 2/95 156/643

PROCESS FOR FABRICATING SUBMICRON SINGLE CRYSTAL ELECTROMECHANICAL STRUCTURES

5,373,627 Grebe; 12/94 29/841
METHOD OF FORMING MULTI-CHIP MODULE WITH HIGH DENSITY INTERCONNECTIONS

5,312,456 Reed, et al.; 5/94 411/456
MICROMECHANICAL BARB AND METHOD FOR MAKING SAME

5,278,442 Prinz, et al.; 1/94 257/417
ELECTRONIC PACKAGES AND SMART STRUCTURES FORMED BY THERMAL SPRAY DEPOSITION

5,258,097 Mastrangelo; 11/93 156/644
DRY-RELEASE METHOD FOR SACRIFICIAL LAYER MICROSTRUCTURE FABRICATION

5,236,118 Bower, et al.; 8/93 228/193
ALIGNED WAFER BONDING

4,953,834 Ebert, et al.; 9/90 267/160
PENDULUM WITH BENDING SPRING JOINT

4,918,032 Jain, et al.; 4/90 437/228
METHOD FOR FABRICATING THREE-DIMENSIONAL MICROSTRUCTURES AND A HIGH SENSITIVITY VIBRATION SENSOR USRING SUCH MICROSTRUCTURES

4,740,410 Muller, et al.; 4/88 428/133
MICROMECHANICAL ELEMENTS AND METHODS FOR THEIR FABRICATION

4,522,893 Bohlen, et al.; 6/85 428/641
CONTACT DEVICE FOR RELEASABLY CONNECTING ELECTRICAL COMPONENTS

GROUP 6: PCT/US96/08274, filed 28 May 96 **[C-15-PCT]**

5,476,211 (See above. commonly-owned patent)

4,674,671 Fister, et al.; 6/87 228/111
THERMOSONIC PALLADIUM LEAD WIRE BONDING

2,429,222 Erhardt, et al.; 10/47 29/885
METHODS OF MAKING CONTACT WIRES

5,228,862 Baumberger, et al.; 7/93 439/66
FLUID PRESSURE ACTUATED CONNECTOR

5,294,039 previously disclosed

GROUP 7: PCT/US96/08276, filed 28 May 96 **[C-16-PCT]**

5,476,211 (See above. commonly-owned patent)

4,674,671 Fister, et al.; 6/87 228/111
THERMOSONIC PALLADIUM LEAD WIRE BONDING

5,495,667 Farnworth, et al.; 3/96 29/843
METHOD FOR FORMING CONTACT PINS FOR SESMICONDUCTOR DICE AND INTERCONNECTS (**note: filing date is 07 Nov 94**)

2,429,222 Erhardt, et al.; 10/47 29/885
METHODS OF MAKING CONTACT WIRES

5,294,039 previously disclosed

GROUP 8A: Database Search

PCT/US95/07901 Fjelstad, et al.; 6/95
(earliest priority date is 6/95)
MICROELECTRONIC CONTACTS AND ASSEMBLIES

PCT/US95/09201 DiStefano, et al.; 7/95
(earliest priority date is 7/94)
ELECTRICAL CONNECTIONS WITH DEEFORMABLE CONTACTS

PCT/US95/11933 Kovac, et al.; 9/95
(earliest priority date is 9/94)
COMPLIANT INTERFACE FOR A SEMICONDUCTOR CHIP

PCT/US96/06228 Fjelstad, et al.; 5/96
(earliest priority date is 5/94)
FABRICATION OF LEADS ON SEMICONDUCTOR CONNECTION COMPONENTS

5,548,091 DiStefano, et al.; 8/96 174/260
SEMICONDUCTOR CHIP CONNECTION COMPONENTS WITH ADHESIVES AND METHODS FOR BONDING TO THE CHIP **(filed 10/93)**

5,557,501 DiStefano, et al.; 9/96 361/704
COMPLIANT THERMAL CONNECTORS AND ASSEMBLIES INCORPORATING THE SAME **(filed Nov. 18, 1994)**

5,597,470 Karavakis, et al.; 1/97 205/118
METHOD FOR MAKING A FLEXIBLE LEAD FOR A MICROELECTRONIC DEVICE **(filed 6/95)**

5,590,460 DiStefano, et al.; 1/97 29/830
METHOD OF MAKING MULTILAYER CIRCUIT **(filed 7/94)**

5,536,909 DiStefano, et al.; 7/96 174/261
SEMICONDUCTOR CONNECTION COMPONENTS AND METHODS WITH RELEASABLE LEAD SUPPORT **(continuation of 919,772 filed 7/92)**

5,558,928 DiStefano, et al.; 9/96 428/209
MULTI-LAYER CIRCUIT STRUCTURES, METHODS OF MAKING SAME AND COMPONENTS FOR USE THEREIN **(division of 815,401 filed 12/91)**

5,570,504 DiStefano, et al.; 11/96 29/830
MULTI-LAYER CIRCUIT CONTSTRUCTION METHOD AND STRUCTURE **(division of 816,634 filed 12/91)**

5,558,321 DiStefano, et al.; 12/96 174/264
MULTI-LAYER CIRCUIT CONSTRUCTION METHODS AND STRUCTURES WITH CUSTOMIZATION FEATURES AND COMPONENTS FOR USE THEREON **(division of 816,634 filed 12/92)**

Attorney Docket No. c-6-us c-6-us.id7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventor(s): Eldridge, et al.

Serial No.: 08/554,902

Filing Date: 11/09/95

SUPPLEMENTAL INFORMATION DISCLOSURE CITATION
(Substitute PTO-1449)

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION (7) is being provided in addition to:

(1) INFORMATION DISCLOSURE CITATION, filed 4/4/96
(2) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(3) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(4) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(5) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 7/17/96
(6) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed herewith

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

Attention is directed to the following commonly-owned patents, **copies of which are enclosed herewith:**

5,476,211 Khandros; 12/95 228/180.5
METHOD OF MANUFACTURING ELECTRICAL CONTACTS, USING A SACRIFICIAL MEMBER

5,601,740 Eldridge, et al.; 2/97 219/130.4
METHOD AND APPARATUS FOR WIREBONDING, FOR SEVERING BOND WIRES, AND FOR FORMING BALLS ON THE ENDS OF BOND WIRES

SOURCE OF THE REFERENCES

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION lists United States Patent No. 5,495,667 and "references cited" therein. Please take note that USP 5,495,667 was filed on November 7, 1994.

___ Copies of the references cited herein are enclosed herewith.

_x_ Copies of the references cited herein may be located in the file of commonly-owned, copending USSN 08/340,144 **[C-2-US]**.

SHOULD THE EXAMINER DESIRE COPIES OF ANY REFERENCES CITED HEREIN, OR IN PREVIOUS INFORMATION DISCLOSURE CITATIONS, APPLICANT WILL PROVIDE SAME UPON REQUEST.

U.S. Patent References:

5,495,667 Farnworth, et al.; 3/96 29/843
METHOD FOR FORMING CONTACT PINS FOR SEMICONDUCTOR DICE AND INTERCONNECTS **(filing date of this patent is 07 Nov 94)**

5,366,589 Chang; 11/94 156/657
BONDING PAD WITH CIRCULAR EXPOSED AREA AND METHOD THEREOF

5,302,891 Wood, et al.; 4/94 324/158 F
DISCRETE DIE BURN-IN FOR NON-PACKAGED DIE

5,293,073 Ono; 3/94 257/740
ELECTRODE STRUCTURE OF A SEMICONDUCTOR DEVICE WHICH USES COPPER WIRE AS A BONDING WIRE

5,266,912 Kledzik; 11/93 333/247
INHERENTLY IMPEDANCE MATCHED MULTIPLE INTEGRATED CIRCUIT MODULE

4,877,173 Fujimoto, et al.; 10/89 228/1.1
WIRE BONDING APPARATUS

4,873,123 Canestaro, et al.; 10/89 427/96
FLEXIBLE ELECTRICAL CONNECTOIN AND METHOD OF MAKING SAME

4,434,347 Kurtz, et al.; 2/84 219/56.22
LEAD FRAME WIRE BONDING BY PREHEATING

4,060,828 Satonaka; 11/77 357/71
SEMICONDUCTOR DEVICE HAVING MULTI-LAYER STRUCTURE WITH ADDITIONAL THROUGH-HOLE INTERCONNECTION

3,894,671 Kulicke, Jr., et al.; 7/75 228/4.5
SEMICONDUCTOR WIRE BONDER

3,381,081 Schalliol; 4/68 174/68.5
ELECTRICAL CONNECTION AND METHOD OF MAKING THE SAME

3,266,137 DeMille, et al.; 8/66 29/473.1
METAL BALL CONNECTION TO CRYSTALS

3,227,933 Punte, et al.; 1/66 317/234
DIODE AND CONTACT STRUCTURES

3,006,067 Anderson, et al.; 10/61 29/470
THERMO-COMPRESSION BONDING OF METAL TO SEMICONDUCTORS AND THE LIKE

Foreign Patent References

58-9330 Japan; 1/83 437/8

Attorney Docket No. c-6-us c-6-us.id8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title: PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventor(s): Eldridge, et al.

Serial No.: 08/554,902

Filing Date: 11/09/95

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(4) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
(5) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 7/17/96
(6) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed herewith
(7) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed herewith

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METHOD OF MANUFACTURING ELECTRICAL CONTACTS, USING A SACRIFICIAL MEMBER

5,601,740 Eldridge, et al.; 2/97 219/130.4
METHOD AND APPARATUS FOR WIREBONDING, FOR SEVERING BOND WIRES, AND FOR FORMING BALLS ON THE ENDS OF BOND WIRES

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SOURCE OF THE REFERENCES

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION lists references discovered in the course of searching the prior art and are arranged in "Groups", as follows:

GROUP 1

_x_ Copies of the references cited herein are enclosed herewith.

___ Copies of the references cited herein may be located in the file of commonly-owned, copending 08/554,902 **[C-6-US]**

U.S. Patent References:

5,461,327	Shibata et al.; 10/95	324/760

PROBE APPARATUS

5,436,571	Karasawa; 7/95	324/765

PROBING TEST METHOD OF CONTACTING A PLURALITY OF PROBES OF A PROBE CARD WITH PADS ON ACHIP ON A SEMICONDUCTOR WAFER

5,422,579	Yamaguchi; 6/95	324/758

METHOD OF IDENTIFYING PROBE POSITION AND PROBING METHOD IN PROBER

5,412,329	Iino et al.; 5/95	324/754

PROBE CARD

5,410,259	Fujihara et al.; 4/95	324/758

PROBING DEVICE SETTING A PROBE CARD PARALLEL

5,399,983	Nagasawa; 3/95	324/758

PROBE APPARATUS

5,378,971	Yamashita; 1/95	324/760

PROBE AND A METHOD OF MANUFACTURING THE SAME

5,325,052	Yamashita; 6/94	324/158P

PROBE APARATUS

5,321,453	Mori et al.; 6/94	324/158 P

PROBE APPARATUS FOR PROBING AN OBJECT HELD ABOVE THE PROBE CARD

5,321,352	Takebuchi; 6/94	324/158 F

PROBE APARATUS AND METHOD OF ALIGNMENT FOR THE SAME

5,278,494 Obigane; 1/94 324/158 F
WAFER PROBING TEST MACHINE

5,266,895 Yamashita; 11/93 324/158 P
PROBE WITH CONTACT PORTION INCLUDING AU AND CU ALLOY
5,220,279

5,198,755 Ikeda et al.; 3/93 324/158 P
PROBE APPARATUS
5,172,053 Itoyama; 12/92 324/158 F
PROBER APPARATUS

5,166,603 Hoshi; 11/92 324/158 P
PROBE METHOD

5,151,651 Shibata; 9/92 324/158 P
APPARATUS FOR TESTING IC ELEMENTS

5,126,662 Jinbo; 6/92 324/158 P
METHOD OD TESTING A SEMICONDUCTOR CHIP

5,113,132 Hoshi; 6/92 324/158 F
PROBING METHOD

5,091,694 Ikeda et al.; 2/92 324/158 P
QUARTZ PROBE APPARATUS

5,091,692 Ohno et al.; 2/92 324/158 F
PROBING TEST DEVICE

5,086,270 Karasawa et al.; 2/92 324/158 P
PROBE APPARATUS

5,061,894 Ikeda; 10/91 324/158 F
PROBE DEVICE

5,034,684 Mitsui et al.; 7/91 324/158 F
PROBE DEVICE AND METHOD OF CONTROLLING THE SAME

4,998,062 Ikeda; 3/91 324/158 F
PROBE DEVICE HAVING MICRO-STRIP LINE STRUCTURE

4,985,676 Karasawa; 1/91 324/158 R
METHOD AND APPARATUS OF PERFORMING PROBING TEST FOR ELECTRICALLY AND SEQUENTIALLY TESTING SEMICONDUCTOR DEVICE PATTERNS

4,965,515 Karasawa; 10/90 324/158 R
APPARATUS AND METHOD OF TESTING A SEMICONDUCTOR WAFER

4,950,982 Obikane et al.; 8/90 324/158 F
ELECTRIC PROBING TEST MACHINE

4,943,767 Yokota; 7/90 324/158 F
AUTOMATIC WAFER POSITION ALIGNING METHOD FOR WAFER PROBER

4,901,011 Koike et al.; 2/90 324/158 F
CARRIER FOR TRANSFERRING PLATE-LIKE OBJECTS ONE BY ONE, A HANDLING APPARATUS FOR LOADING OR UNLOADING THE CARRIER, AND A WAFER PROBING MACHINE FITTED WITH THE HANDLING APPARATUS FOR THE WAFER CARRIER

4,875,005 Terada et al.; 10/89 324/158 F
MECHANISM FOR TURNING OVER A TEST HEAD OF A WAFER PROBING MACHINE

4,604,910 Chadwick et al.; 8/86 74/96
APPARATUS FOR ACCURATELY POSITIONING AN OBJECT AT EACH OF TWO LOCATIONS

4,123,706 Roch; 10/78 324/158 P
PROBE CONSTRUCTION

4,056,777 Roch; 11/77 324/158 P
MICROCIRCUIT TEST DEVICE WITH MULTI-AXES PROBE CONTROL

4,034,293 Roch; 7/77 324/158 P
MICRO-CIRCUIT TEST PROBE

4,001,685 Roch; 1/77 324/158 P
MICRO-CIRCUIT TEST PROBE

3,940,676 Dudley; 2/76 318/612
DAMPING CONTROL FOR POSITIONING APPARATUS

3,939,414 Roch; 2/76 324/158 F
MICRO-CIRCUIT TEST APPARATUS

GROUP 2
REFERENCES HAVING GENERAL INTEREST

___ Copies of the references cited herein are enclosed herewith.

_x_ Copies of the references cited herein may be located in the file of commonly-owned, copending USSN 08/558,332 **[C-7-US]**

5,570,032 Atkins, et al.; 10/96 324/760
WAFER SCALE BURN-IN APPARATUS AND PROCESS

5,532,610 Tsujide, et al.; 7/96 324/757
APPARATUS FOR TESTING SEMICONDUCTOR WAFER

5,497,079 Yamada, et al.; 3/96 324/158.1
SEMICONDUCTOR TESTING APPARATUS, SEMICONDUCTOR TESTING CIRCUIT CHIP, AND PROBE CARD

5,434,513 Fujii, et al.; 7/95 324/765
SEMICONDUCTOR WAFER TESTING APPARATUS USING INTERMEDIATE SEMICONDUCTOR WAFER

5,073,117 Malhi, et al.; 12/91 439/71
FLIP-CHIP SOCKET ADAPTOR AND METHOD

4,899,107 Corbett, et al.; 2/90 324/158F
DISCRETE DIE BURN-IN FOR NONPACKAGED DIE

GROUP 3
INTERFACES BETWEEN THE WAFER AND THE TESTER

___ Copies of the references cited herein are enclosed herewith.

_x_ Copies of the references cited herein may be located in the file of commonly-owned, copending USSN 08/558,332 **[C-7-US]**

3A. Of seemingly greater relevance

5,070,297 Kwon, et al.; 12/91 324/158 P
FULL WAFER INTEGRATED CIRCUIT TESTING DEVICE

5,457,400 Ahmad, et al.; 10/95 324/763
SEMICONDUCTOR ARRAY HAVING BUILT-IN TEST CIRCUIT FOR WAFER LEVEL TESTING

5,397,997 Tuckerman, et al.; 3/95 324/754
BURN-IN TECHNOLOGIES FOR UNPACKED INTEGRATED CIRCUITS

5,461,328 Devereaux, et al.; 10/95 324/765
FIXTURE FOR BURN-IN TESTING OF SEMICONDUCTOR WAFERS

5,446,395 Goto; 8/95 324/763
TEST CIRCUIT FOR LARGE SCALE INTEGRATED CIRCUITS ON A WAFER

5,483,175 Ahmad, et al.; 1/96 324/766
METHOD FOR CIRCUITS CONNECTION FOR WAFER LEVEL BURNING AND TESTING OF INDIVIDUAL DIES ON SEMICONDUCTOR WAFER

5,336,992 Saito,et al.; 8/94 324/754
ON-WAFER INTEGRATED CIRCUIT ELECTRICAL TESTING

5,532,614 Chiu; 7/96 324/763
WAFER BURN-IN AND TEST SYSTEM

5,055,780 Takagi, et al.; 10/91 324/158
PROBE PLATE USED FOR TESTING A SEMICONDUCTOR DEVICE, AND A TEST APPARATUS THEREFOR

5,047,711 Smith, et al.; 9/91 324/158R
WAFER-LEVEL BURN-IN TESTING OF INTEGRATED CIRCUITS

5,440.241 King, et al.; 8/95 324/765
METHOD FOR TESTING, BURNING-IN, AND MANUFACTURING WAFER SCALE INTEGRATED CIRCUITS AND A PACKAGED WAFER ASSEMBLY PRODUCED THEREBY

3B. Of seemingly lesser relevance

5,479,109 Lau, et al.; 12/95 324/758
TESTING DEVICE FOR INTEGRATED CIRCUITS ON WAFER

5,444,386 Mizumura; 8/95 324/754
PROBING APPARATUS HAVING AN AUTOMATIC PROBE CARD INSTALL MECHANISM AND A SEMICONDUCTOR WAFER TESTING SYSTEM INCLUDING THE SAME

5,442,282 Rostoker, et al.; 8/95 324/158.1
TESTING AND EXERCISING INDIVIDUAL, UNSINGULATED DIES ON A WAFER

5,391,984 Worley; 2/95 324/158.1
METHOD AND APPARATUS FOR TESTING INTEGRATED CIRCUIT DEVICES

5,363,038 Love; 11/94 324/158.1
METHOD AND APPARATUS FOR TESTING AN UNPOPULATED CHIP CARRIER USING A MODULE TEST CARD

4,038,599 Bove, et al.; 7/77 324/158 F
HIGH DENSITY WAFER CONTACTING AND TEST SYSTEM

3,849,872 Hubacher; 11/74 29/574
CONTACTING INTEGRATED CIRCUIT CHIP TERMINAL THROUGH THE WAFER

GROUP 4: Flat Probes

___ Copies of the references cited herein are enclosed herewith.

_x_ Copies of the references cited herein may be located in the file of commonly-owned, copending USSN 08/558,332 **[C-7-US]**

4A. Of seemingly greater relevance

5,555,422 Nakano; 9/96 324/754
PROBER FOR SEMICONDUCTOR INTEGRATED CIRCUIT ELEMENT WAFER

5,517,126 Yamaguchi; 5/96 324/758
PROBE APPARATUS

5,444,366 Chiu; 8/95 324/158.1
WAFER BURN-IN AND TEST SYSTEM

5,510,724 Itoyama, et al.; 4/96 324/760
PROBE APPARATUS AND BURN-IN APPARATUS

5,559,446 Sano; 9/96 324/760
PROBING METHOD AND DEVICE

5,389,873 Ishii, et al.; 2/95 324/158.1
PRESSURE CONTACT CHIP AND WAFER TESTING DEVICE

5,550,482 Sano; 8/96 324/758
PROBE DEVICE

5,424,651 Green, et al.; 6/95 324/754
FIXTURE FOR BURN-IN TESTING OF SEMICONDUCTOR WAFERS, AND A SEMICONDUCTOR WAFER

4B. Of seemingly lesser relevance

5,585,737 Shibata 324/754
SEMICONDUCTOR WAFER PROBING METHOD...

5,534,784 Lum, et al.; 7/96 324/757
METHOD FOR PROBING A SEMICONDUCTOR WAFER

5,506,498 Anderson, et al.; 4/96 324/158.1
PROBE CARD SYSTEM AND METHOD

5,436,571 Karasawa; 7/95 324/765
PROBING TEST METHOD OF CONTACTING A PLURALITY OF PROBES OF A PROBE CARD WITH PADS ON A CHIP ON A SEMICONDUCTOR WAFER

5,338,223 Melatti, et al.; 8/94 439/482
HYBRID WAFER PROBE

5,220,277 Reitinger; 6/93 324/158 F
ARRANGEMENT FOR TESTING SEMICONDUCTOR WAFERS OR THE LIKE

5,1330,644 Ott; 7/92 324/58 F
INTEGRATED CIRCUIT SELF-TESTING DEVICE AND METHOD

4,961,052 Tada, et al.; 10/90 324/158 P
PROBING PLATE FOR WAFER TESTING

4,899,099 Mendenhall, et al.; 2/90 324/158 F
FLEX DOT WAFER PROBE

4,780,836 Miyazaki, et al.; 10/88 364/551.01
METHOD OF TESTING SEMICONDUCTOR DEVICES USING A PROBE CARD

4,727,3319 Shahriary; 2/88 324/158 P
APPARATUS FOR ON-WAFER TESTING OF ELECTRICAL CIRCUITS

GROUP 5: Temperature-controlled or flat chucks

___ Copies of the references cited herein are enclosed herewith.

_x_ Copies of the references cited herein may be located in the file of commonly-owned, copending USSN 08/558,332 **[C-7-US]**

5A. Of seemingly greater relevance

5B. Of seemingly lesser relevance

5,532,609 Harwood, et al.; 7/96 324/754
WAFER PROBE STATION HAVING ENVIRONMENT CONTROL ENCLOSURE

5,457,398 Schwindt, et al.; 10/95 324/754
WAFER PROBE STATION HAVING FULL GUARDING

5,325,052 Yamashita; 6/94 324/158 P
PROBE APPARATUS

5,303,938 Miller, et al.; 4/94 279/3
KELVIN CHUCK APPARATUS AND METHOD OF MANUFACTURE

5,266,889 Harwood, et al.; 324/158 F
WAFER PROBE STATION WITH INTEGRATED ENVIRONMENT CONTROL ENCLOSURE

5,198,752 Miyata, et al.; 3/93 324/158 F
ELECTRIC PROBING-TEST MACHINE HAVING A COOLING SYSTEM

GROUP 6: Probe Structure or spring structure

___ Copies of the references cited herein are enclosed herewith.

_x_ Copies of the references cited herein may be located in the file of commonly-owned, copending USSN 08/558,332 **[C-7-US]**

6A. Of seemingly greater relevance

6B. Of seemingly lesser relevance

5,247,250 Rios; 9/93 324/158 F
INTEGRATED CIRCUIT TEST SOCKET

5,214,375 Ikeuchi, et al.; 5/93 324/158 P
MULTI-POINT PROBE ASSEMBLY FOR TESTING ELECTRONIC DEVICE

4,998,062 Ikeda; 3/91 324/158 F
PROBE DEVICE HAVING MICRO-STRIP LINE STRUCTURE

4,985,676 Karasawa; 1/91 324/158 R
METHOD AND APPARATUS OF PERFORMING PROBING TEST...

4,870,356 Tingley; 9/89 324/158 F
MULTI-COMPONENT TEST STRUCTURE

4,523,144 Okubo, et al.; 6/85 324/158 P
COMPLEX PROBE CARD FOR TESTING A SEMICONDUCTOR WAFER

GROUP 7: Other patents of interest

___ Copies of the references cited herein are enclosed herewith.

_x_ Copies of the references cited herein may be located in the file of commonly-owned, copending USSN 08/558,332 **[C-7-US]**

7A. Of seemingly greater relevance

5,534,786 Kaneko, et al.; 7/96 324/760
BURN-IN AND TEST METHOD OF SEMICONDUCTOR WAFERS AND BURN-IN BOARDS FOR USE IN SEMICONDUCTOR WAFER BURN-IN TESTS

5,479,108 Cheng; 12/95 324/765
METHOD AND APPARATUS FOR HANDLING WAFERS

7B. Of seemingly lesser relevance

5,568,056 Ishimoto; 10/96 324/754
WAFER PROBER

5,559,444 Farnworth, et al.; 9/96 324/754
METHOD AND APPARATUS FOR TESTING UNPACKAGED SEMICONDUCTOR DICE

5,488,292 Tsuta; 1/96 324/158.1
WAFER INSPECTING SYSTEM

5,410,162 Tigelaar, et al.; 4/95 257/48
APPARATUS FOR AND METHOD OF RAPID TESTING OF SEMICONDUCTOR COMPONENTS AT ELEVATED TEMPERATURE

5,355,081 Nakata, et al.; 10/94 324/765
METHOD FOR TESTING A SEMICONDUCTOR INTEGRATED CIRCUIT HAVING SELF TESTING CIRCUIT

5,329,228 Comeau; 7/94 324/765
TEST CHIP FOR SEMICONDUCTOR FAULT ANALYSIS

5,187,020 Kwon, et al.; 2/93 428/601
COMPLIANT CONTACT PAD

5,140,405 King, et al.; 8/92 357/67
SEMICONDUCTOR ASSEMBLY UTILIZING ELASTOMERIC SINGLE AXIS CONDUCTIVE INTERCONNECT

4,764,723 Strid; 8/88 324/158 P
WAFER PROBE

4,746,857 Sakai, et al.; 5/88 324/158 F
PROBING APPARATUS FOR MEASURING ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR DEVICE FORMED ON WAFER

4,697,143 Lockwood, wt al.; 9/87 324/158 P
WAFER PROBE

4,567,433 Ohkubo, et al.; 1/86 324/158 P
COMPLEX PROBE CARD FOR TESTING A SEMICONDUCTOR WAFER